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REMARKS

In the Office Action, the Examiner rejected claims 1-3, 5-7, 15-17 and 19-28 under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (U.S. Patent No. 6,081,026) in view of Akagawa et al. (U.S. Patent No. 5,834,844) and the admitted prior art (APA). The rejection is respectfully traversed. Reconsideration of the application is respectfully requested based on the following remarks.

Claims 1 and 15 have been amended to further clarify the subject matter regarded as the invention. Claims 23, 24, 27, and 28 have been canceled without prejudice or disclaimer. Accordingly, claims 1-3, 5-7, 15-17, 19-22, and 25-26 are now pending in this application.

REJECTION OF CLAIMS UNDER 35 U.S.C. §103(a)

The invention as set forth in amended independent claim 1 generally relates to a solid flexible circuit film conductively attached to an integrated circuit die. Specifically, independent claim 1 requires among other things "a solid flexible dielectric circuit film having a top surface, a bottom surface", and "at least one outer landing formed on the top surface and at least one inner landing formed on the bottom surface" where the "two landings are connected via the routing conductor, which extends laterally within the solid flexible dielectric circuit film". One of the many advantages of having this solid flexible circuit film in the manner claimed is that it decouples stress between an integrated circuit package and other substrates to which it is attached while keeping its own thickness to a bare minimum. Another advantage is that the routing conductor is protected from exposure to the elements as well as to other surfaces since it extends laterally within the solid flexible dielectric circuit film. Likewise, amended independent claim 15 requires a similar limitation as noted for claim 1 above.

On the other hand, the cited reference of Wang et al. does not have the advantage of keeping the size to a bare minimum or protecting the routing conductor as mentioned above because Wang et al. fails to teach or suggest a solid flexible dielectric circuit film in the manner claimed. The Examiner pointed to a flexible dielectric circuit film (FDCF)/interposer (100 in Fig. 1) having a top and bottom surfaces where outer/inner landing/pad are formed on the top/bottom surfaces respectively (inner landing 126 in Fig. 1-3; outer landing/pad – not numerically referenced in Fig. 1-3). However, as shown in Fig. 1-3, interposer (100) has spaces

present in between the cited top and bottom surfaces, particularly in the area surrounding the dielectric layer (110). Also, the routing conductors either run through vias (112, 402) that extend vertically within the FDCF (dielectric layer 110, dielectric substrate 120) or just on the surfaces of the FDCF (Fig. 1-3), but not laterally within the FDCF. As such, the cited (FDCF)/interposer (100) as well as other embodiments of Wang et al. do not teach or suggest a solid FDCF much less two landings that are connected via a routing conductor, which extends laterally within the solid flexible dielectric circuit film. In addition, the interposers described in Wang et al. as a whole are far more complex than those solid FDCF required by amended claims 1 and 15, making them more expensive to manufacture and more susceptible to failure. In light of these differences, it is respectfully submitted that Wang et al., Akagawa et al., or admitted prior art (APA), alone or in combination, do not teach or suggest amended independent claims 1 and 15. Therefore, it is submitted that amended claims 1 and 15 are patentably distinct from the cited references.

Claims 2-3, 5-7, 16-17, 19-22, and 25-26 each depend either directly or indirectly from independent claims 1 and 15 and are therefore respectfully submitted to be patentable over the art of record for at least the reasons set forth above with respect to the independent claims 1 and 15. Additionally, these dependent claims require additional elements that when taken in the context of the claimed invention as a whole, further patentably distinguishes the art of record.

SUMMARY

It is respectfully submitted that all pending claims are allowable and that this case is now in condition for allowance. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

If any additional fees are due in connection with the filing of this Amendment, the Commissioner is authorized to deduct such fees from the undersigned's Deposit Account No. 500388 (Order No. NSC1P181).

Respectfully submitted,
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

1. (Twice Amended) An integrated circuit package comprising:

an integrated circuit die, said integrated circuit die having a top side and a bottom side opposite said top side, said top side including at least one bond pad;

at least one raised interconnect located over and conductively coupled to said at least one bond pad; and**[**,**]**

a **solid** flexible dielectric circuit film having a top surface, a bottom surface and a routing conductor, the flexible circuit film having at least one outer landing formed on the top surface and at least one inner landing formed on the bottom surface such that the landings on the top **and bottom** surfaces **[**is**]** **are** fully supported by the **[underlying]** circuit film **[and the landing on the bottom surface is fully supported by the overlying circuit film]**, wherein the outer landing is laterally offset from the inner landing and the two landings are connected via the routing conductor**, which extends laterally within the solid flexible dielectric circuit film**,

wherein the flexible circuit film being located over and conductively attached to at least one raised interconnect such that an air gap is formed between said integrated circuit die and said flexible circuit film.

15. (Twice Amended) An integrated circuit wafer having a top side and a bottom side opposite said top side, said integrated circuit wafer comprising:

a plurality of integrated circuit dice, said plurality of integrated circuit dice having a plurality of bond pads located on said top side of said integrated circuit wafer;

a plurality of raised interconnects formed over and conductively coupled to said plurality of bond pads; and**[,]**

a **solid** flexible dielectric circuit film having a top surface, a bottom surface and routing conductors, the flexible circuit film having a plurality of outer landings located on the top surface and a plurality of inner landings located on the bottom surface such that the landings on the top **and bottom** surface**s** are fully supported by the **[underlying]** circuit film **[and the landings on the bottom surface are fully supported by the overlying circuit film]**, wherein the individual outer landings are laterally offset from the individual inner landings and the landings are connected via routing conductors**, which extend laterally within the solid flexible dielectric circuit film**,

wherein the flexible circuit film being located over and conductively attached to the plurality of raised interconnects such that an air gap is formed between said integrated circuit wafer and said flexible circuit film.